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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,591	10/16/2003	Koichi Yamamoto	Q78025	5122
23373	7590	01/25/2005		
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER BENSON, WALTER	
			ART UNIT 2858	PAPER NUMBER

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,591

Applicant(s)

YAMAMOTO, KOICHI

Examiner

Walter Benson

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2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on IDS filed 10/16/03.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6 and 7 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/16/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are presented for examination.

Specification

2. The abstract of the disclosure is objected to because it unclear what is meant by “low level which are appeared repeatedly” lines 5-6; and “ground fault is occurred” line 13.

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

page 9, line 24, “ground fault ‘ is misspelled.

Appropriate correction is required.

Claim Objections

4. Claims 1 and 7 are objected to because of the following informalities:

Claim 1, line 4, it is unclear what is meant by “which are appeared repeatedly”

Claim 7, line 2, “fault is occurred” should read –fault has occurred--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4 and 6-7 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US 2002/0121902 A1 and Suzuki hereinafter) in view of Engel (US Patent No. 4,180,841 and Engel hereinafter).

7. As to claims 1-4, 6 and 7, Suzuki discloses a ground-fault detecting device substantially as claimed, comprising:

a power source electrically insulated from a vehicle body {claims 1,6} [0034];

a pulse signal generator, generating a pulse signal having a high level and a low level

which are appeared repeatedly in a prescribed cycle {claims 1,6} ([0036], lines 3-5);

a detection resistor, connected to the pulse signal generator and the power source {claims 1,6} ([0036], lines 5-6);

a coupling capacitor, connected to the detecting resistor in series {claims 1, 6}([0036], lines 7-8);

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where the ground-fault determinant is a sample-and-hold circuit which sample-and-holds the output of the integrator as an integration value for obtaining a ground-fault detection output {claim 4} ([0039], lines 9-13);

an insulation resistance, electrically insulating the power source from a vehicle body {claim 6} ([0043], Lines 6-8);

an A/D converter, A/D converting an output of the integrator [i.e. Laplace Transform] as integration value so as to generate a digital value corresponding to a resistance value of the insulation resistance {claim 6} [0039].

Suzuki did not expressly disclose:

an integrator, integrating a difference between a first reference voltage and a detection voltage of the pulse signal at a connecting point of the detection resistor and the coupling capacitor over an integration interval {claims 1,6};

a ground-fault determinant, judging whether a ground fault is occurred on the basis of an output of the integrator {claims 1, 7};

where the integration interval has at least pad of a high-level interval and a low-level interval of the pulse signal {claims 1,6};

an integration circuit, integrating the difference between the detection voltage and the first reference voltage {claim 2};

an integration reset signal generation circuit, generating a reset signal for rendering the integration circuit in a reset state over intervals other than the integration interval on the basis of the pulse signal supplied from the pulse signal generator {claim 2};

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ground-fault determinant is a hysteresis comparator which compares the output of the integrator with a second reference voltage for obtaining a ground-fault detection output {claim 3};

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Suzuki, as evidenced by Engel.

Engel discloses ground fault circuit interrupter having:
an integrator, integrating a difference between a first reference voltage and a detection voltage of the pulse signal at a connecting point of the detection resistor and the coupling capacitor over an integration interval {claims 1,6} (col. 4, lines 37-42) to provide a level over the time interval;

a ground-fault determinant, judging whether a ground fault is occurred on the basis of an output of the integrator {claims 1, 7} (col. 4, lines 22-24) when the integrator exceeds a predetermined limit;

where the integration interval has at least pad of a high-level interval and a low-level interval of the pulse signal {claims 1,6} (col. 5, lines 1-4) to provide for each half cycle;

an integration circuit, integrating the difference between the detection voltage and the first reference voltage {claim 2} (col. 4, lines 18-14);

an integration reset signal generation circuit, generating a reset signal for rendering the integration circuit in a reset state over intervals other than the integration interval on the basis of the pulse signal supplied from the pulse signal generator {claim 2} (col. 4, lines 21-22) to detect low resistance paths;

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ground-fault determinant is a hysteresis comparator which compares the output of the integrator with a second reference voltage for obtaining a ground-fault detection output {claim 3} (col. 7, lines 18-20).

Given the teaching of Engel, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Suzuki by employing the well known or conventional features of ground fault circuits, such as disclosed by Engel in order to efficiently alleviate false ground fault outputs.

Allowable Subject Matter

8. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fail to teach in combination as claimed a ground-fault detecting device that includes a compensation capacitor, having a capacitance corresponding to a vehicle-side capacitance, and provided between the vehicle body and the coupling capacitor.

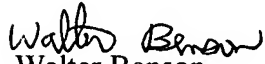
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (571) 272-2227. The examiner can normally be reached on Mon to Fri 6:30 AM to 4:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571) 272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Walter Benson
Patent Examiner

January 20, 2005